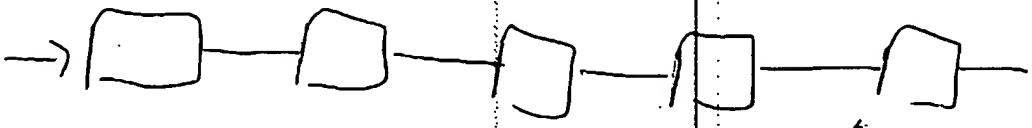
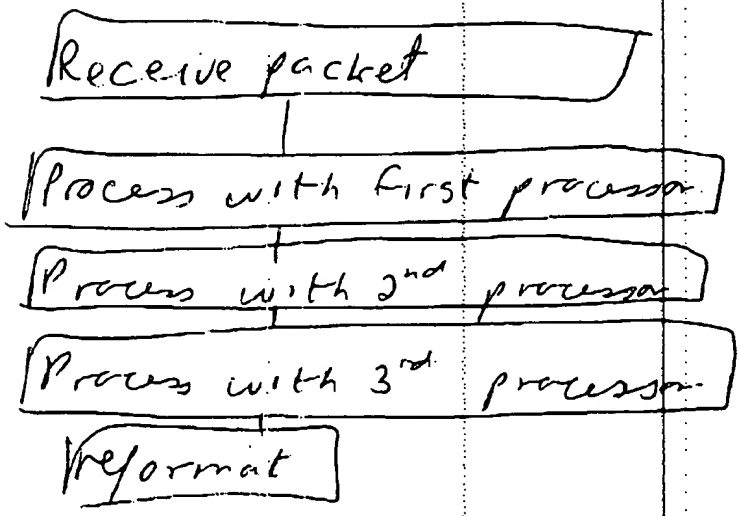


Prior Art

Fig. 1



Prior Art

Fig. 2

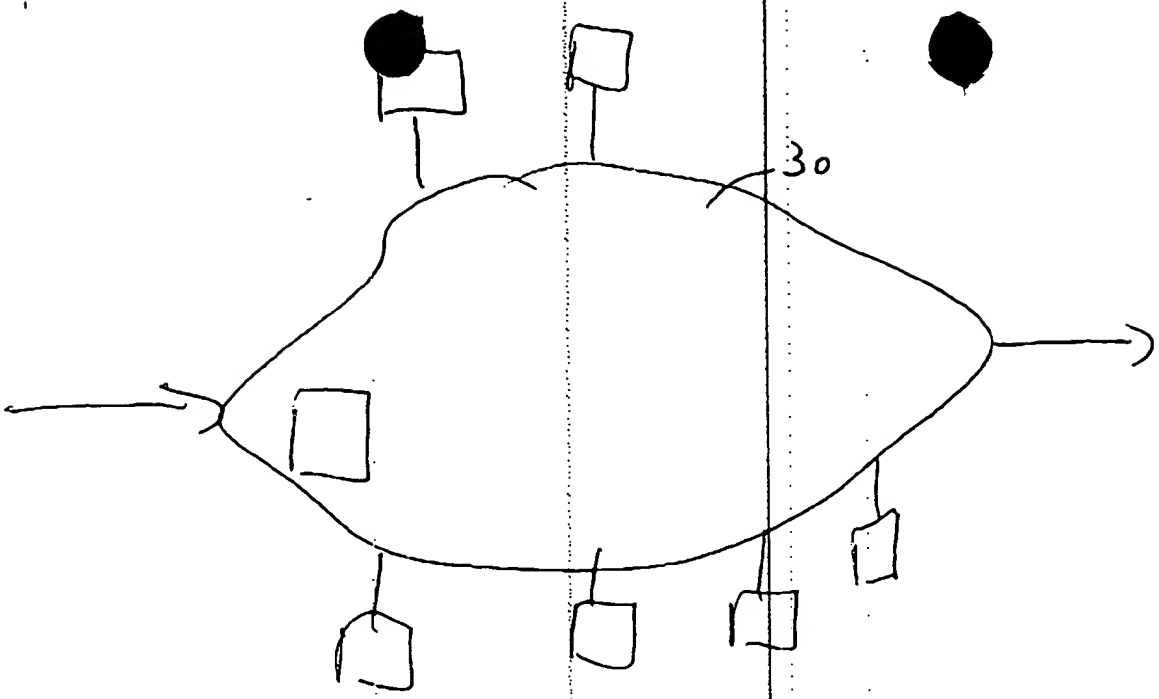


Fig. 3

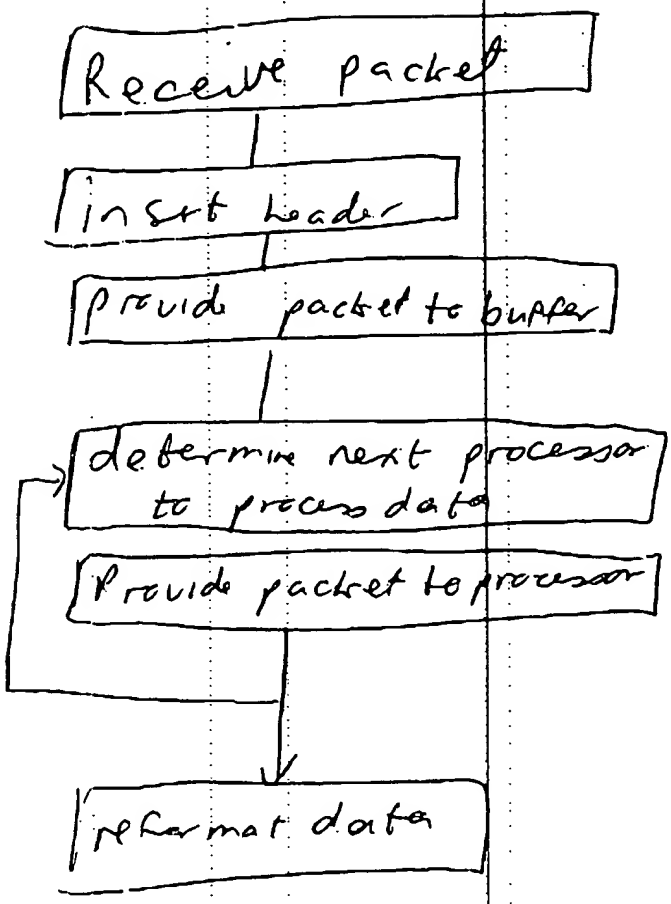

Receive packet
insert header
provide packet to buffer
determine next processor to process data
Provide packet to processor
reformat data

Fig. 4

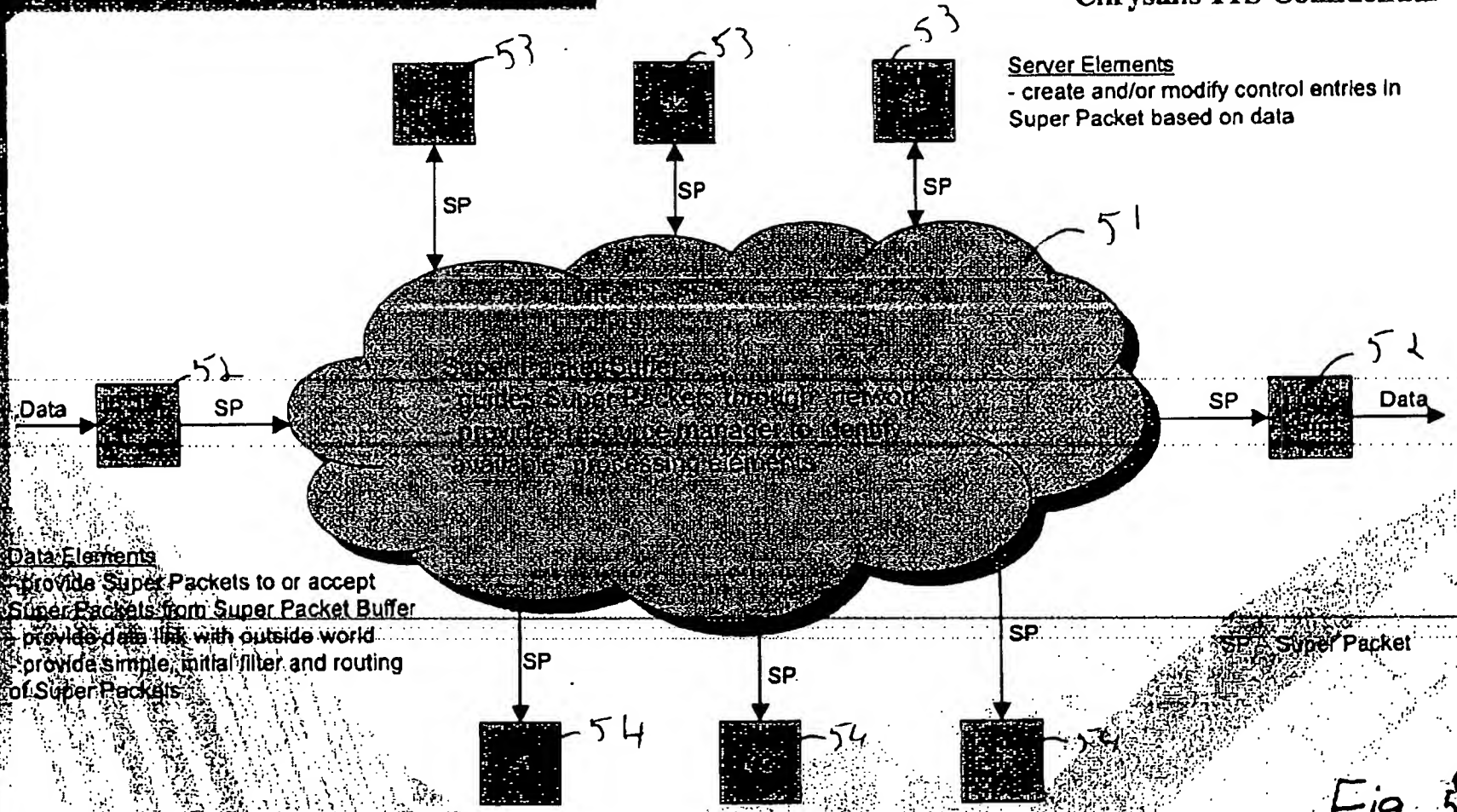


Fig. 5

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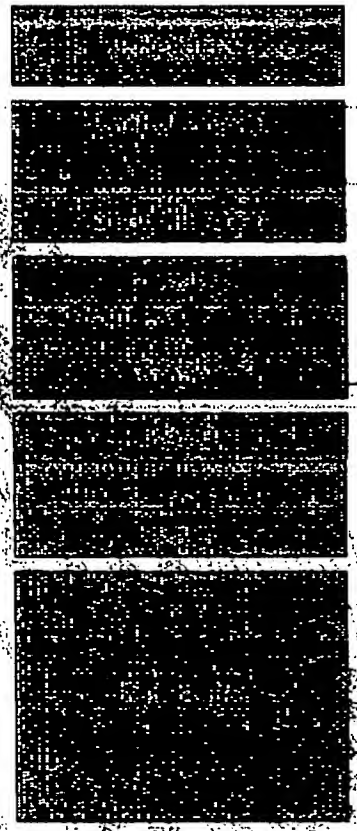
Super Packet

- Contains all control, coding, keying information required to process the contained data



Header identifies Super Packet and provides timing and tracking information.

Control Entries identify operation to be performed on attached data and how to treat result data, result codes and completion information are placed back into the control entries.

uCode is the instructions required by the generic control elements to perform the commands coded in the control entries on the associated data.

Keying information must be provided for each control action that invokes a cryptographic operation.

Data buffer controls original and modified data.

Fig 6

Super Packet Buffer

- Responsible for moving Super Packet between the generic processing elements

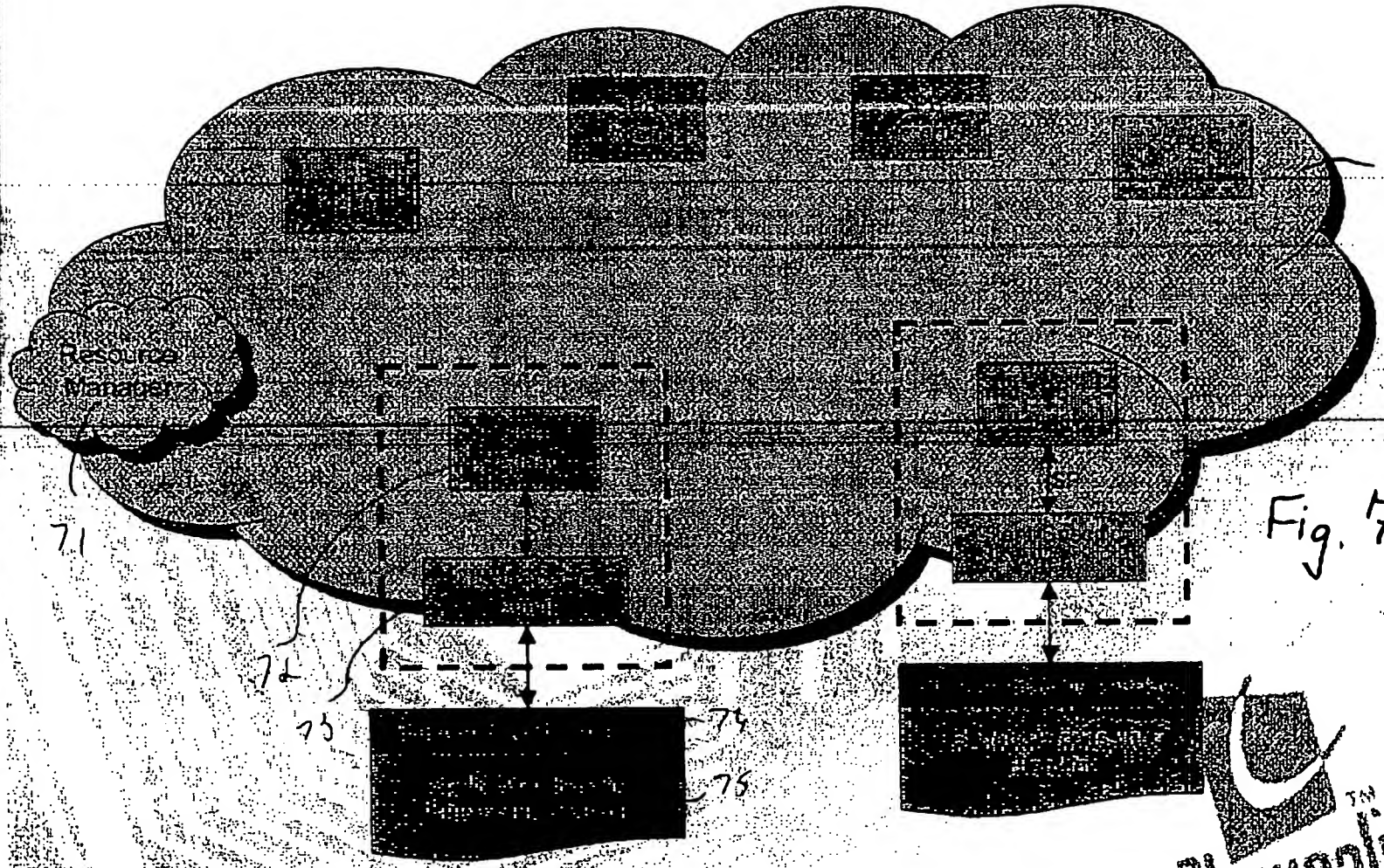


Fig. 7

IPSec Processing Example

(ESP OutBound, Transport Mode)

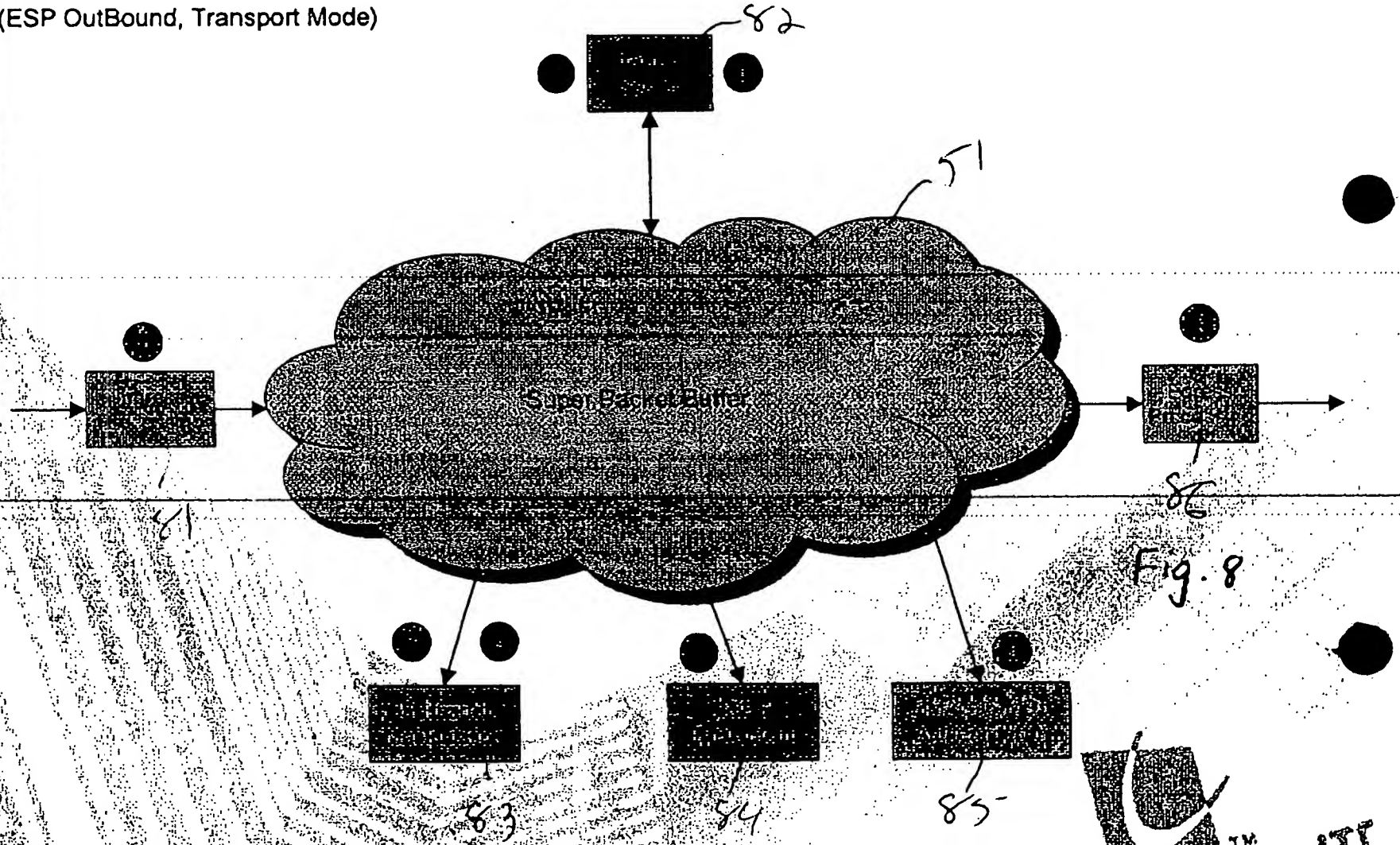
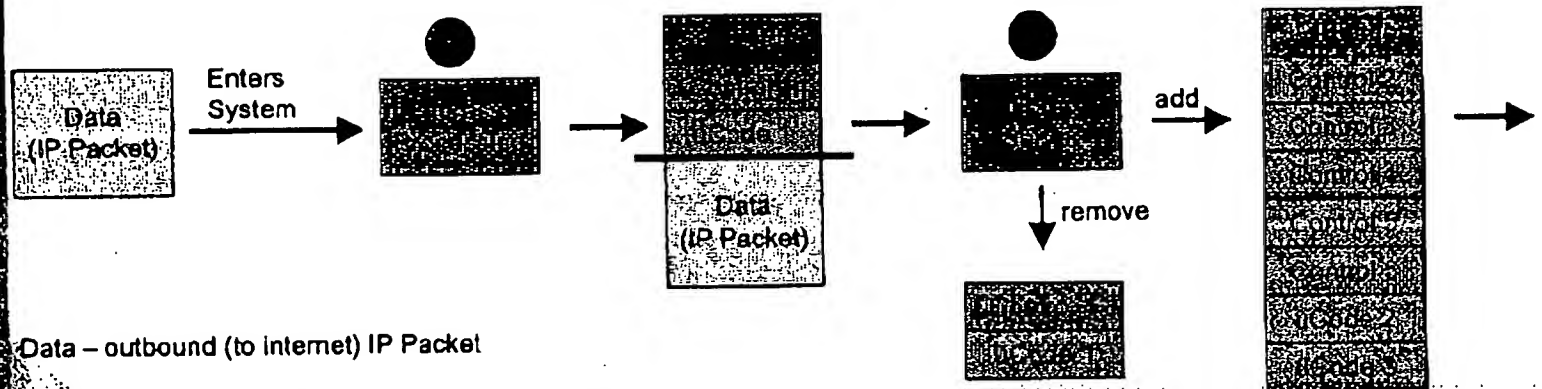


Fig. 8

IPSec Super Packet (1)



Data – outbound (to internet) IP Packet

SP Header – header added to identify super packet

Control 1
Action: Route to IPSec Server Element
uCode 1 : Provide Code identity to process outbound IPSec packet

Control 2
Action: Route to IPSec Header processing element
uCode 2 : Code identity to insert ESP header and trailer

Control 3
Action : Route to 3DES processing element and encrypt
uCode 3 : 3DES algorithm (CBC Mode)
Key 3 : 3DES key for packet

Control 4
Action : Route to HMAC96-MD5 processing element and generate MAC
uCode 4 : HMAC96-MD5 algorithm
Key 4 : HMAC Key for packet

Fig. 9a

Control 5
Action : Place MAC in ESP Header
uCode 5 : Code identify for post encryption header manipulation

Control 6
Action : Route to Egress Unit
uCode 6 : Code identify to strip new IP Packet from Super Packet and transmit

IPSec Super Packet (2)

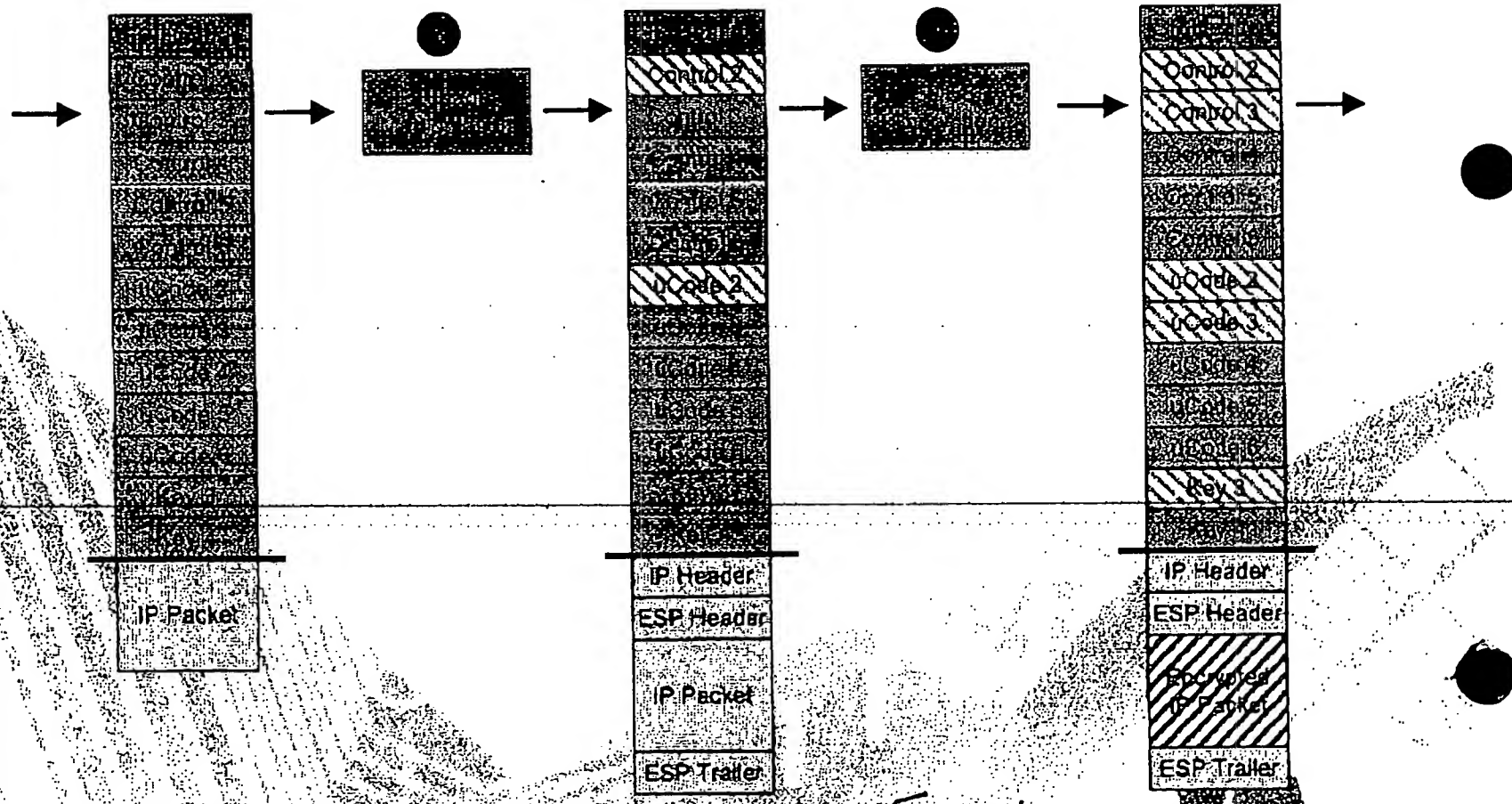


Fig. 9b

Cross hatch indicates processing complete

IPSec Super Packet (3)

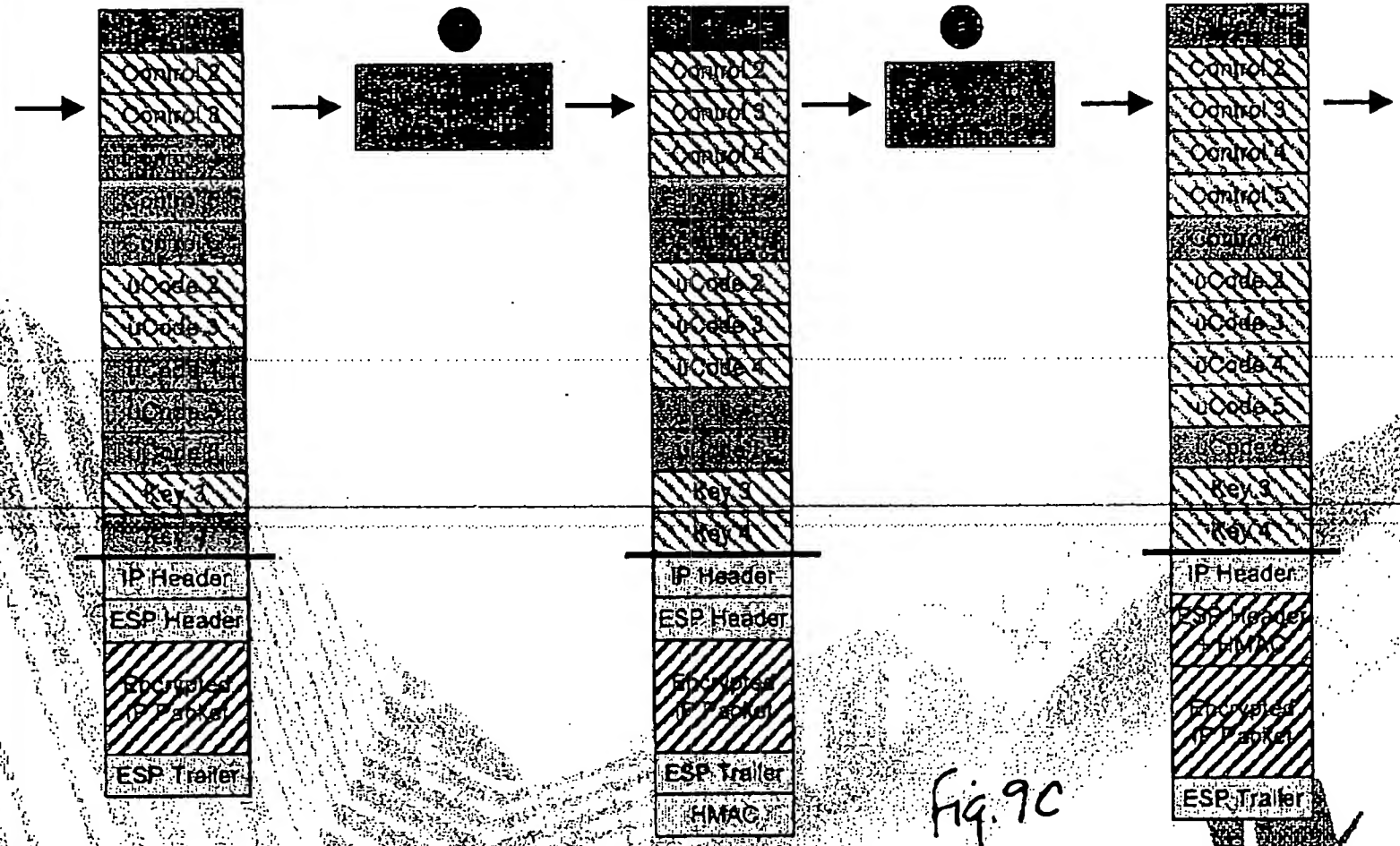
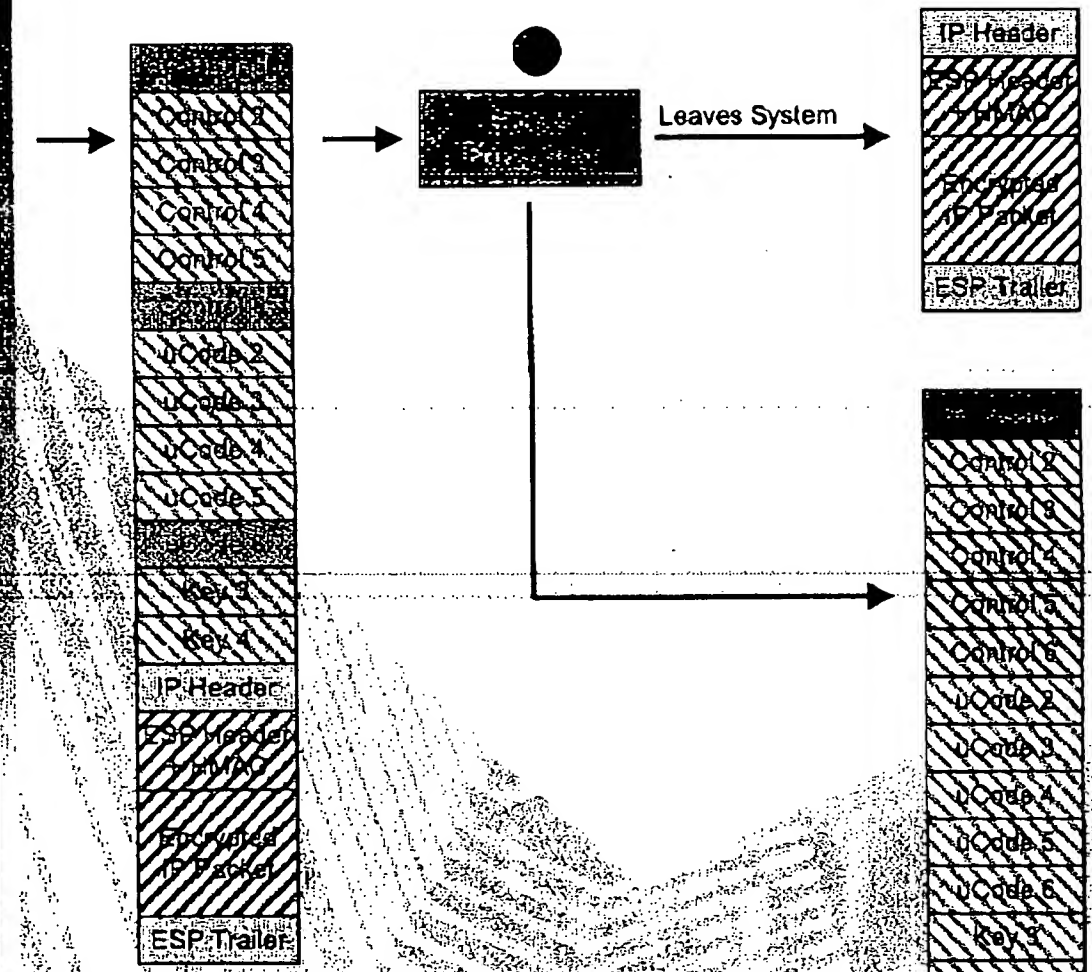


Fig. 9C

Cross hatch indicates processing complete

IPSec Super Packet (4)



Cross hatch indicates processing complete

Fig. 9d

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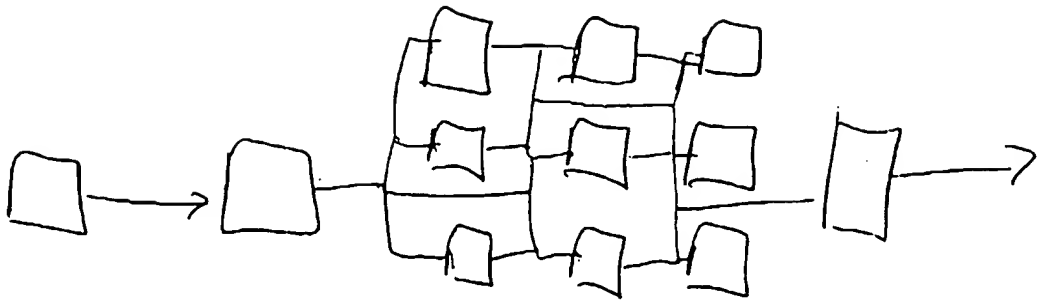

Fig. 10